

Claims

What is claimed is:

- 1 1. A method for implementing high frequency return current paths
2 utilizing decoupling capacitors within electronic packages comprising the
3 steps of:
4 receiving electronic package physical design data for identifying a
5 design layout;
6 utilizing said identified design layout for identifying a respective
7 number of signal vias and a respective number of return current paths for a
8 plurality of cells in a grid of a set cell size within said identified design layout;
9 calculating ratio of signal vias to return current paths for each of said
10 plurality of cells;
11 identifying each cell having said calculated ratio greater than a target
12 ratio; and
13 selectively adding one or more decoupling capacitors within each said
14 identified cell for providing high frequency return current paths.
- 1 2. A method for implementing high frequency return current paths
2 within electronic packages as recited in claim 1 wherein the step of receiving
3 electronic package physical design data for identifying said board layout
4 includes the steps of receiving plane stack-up data for identifying reference
5 voltages residing on multiple planes and for creating pairs of reference
6 voltages to be analyzed.
- 1 3. A method for implementing high frequency return current paths
2 within electronic packages as recited in claim 1 wherein the step of receiving
3 electronic package physical design data for identifying said board layout
4 includes the step of receiving a board file for identifying locations of high
5 speed nets, locations of plane change vias, and board dimensions.
- 1 4. A method for implementing high frequency return current paths
2 within electronic packages as recited in claim 1 includes the step of receiving
3 a user selected value for said target ratio; said target ratio defining a
4 maximum desired ratio of signal vias to return current paths.

1 5. A method for implementing high frequency return current paths
2 within electronic packages as recited in claim 1 includes the step of receiving
3 a user selected grid dimensions input defining said set cell size.

1 6. A method for implementing high frequency return current paths
2 within electronic packages as recited in claim 1 wherein the step of
3 selectively adding one or more decoupling capacitors within each said
4 identified cell for providing high frequency return current paths includes the
5 step of identifying nets referenced to at least one reference voltage within
6 each said identified cell.

1 7. A method for implementing high frequency return current paths
2 within electronic packages as recited in claim 1 wherein the step of
3 selectively adding one or more decoupling capacitors within each said
4 identified cell for providing high frequency return current paths includes the
5 steps of calculating a capacitance value, a capacitor quantity, and optimal
6 placement for adding said one or more decoupling capacitors within said
7 cell.

1 8. A method for implementing high frequency return current paths
2 within electronic packages as recited in claim 1 wherein the step of
3 selectively adding one or more decoupling capacitors within each said
4 identified cell for providing high frequency return current paths includes the
5 steps of identifying nets referenced to at least one reference voltage within
6 each said identified cell; and connecting said one or more decoupling
7 capacitors between at least one ground plane and at least one plane for said
8 at least one reference voltage within said cell.

1 9. A method for implementing high frequency return current paths
2 within electronic packages as recited in claim 1 wherein the step of
3 selectively adding one or more decoupling capacitors within each said
4 identified cell for providing high frequency return current paths includes the
5 steps of identifying nets referenced to at least one reference voltage within
6 each said identified cell; and includes the steps of connecting a first
7 decoupling capacitor between a ground plane and one said reference
8 voltage within said cell; and connecting a second decoupling capacitor
9 between said ground plane and another said reference voltage within said
10 cell.

1 10. A method for implementing high frequency return current paths
2 within electronic packages as recited in claim 9 includes the step of
3 connecting said first decoupling capacitor and said second decoupling
4 capacitor to a plurality of said ground planes.

1 11. A computer program product for implementing high frequency
2 return current paths within electronic packages in a computer system, said
3 computer program product including instructions executed by the computer
4 system to cause the computer system to perform the steps of:
5 receiving electronic package physical design data for identifying a
6 design layout;
7 utilizing said identified design layout for identifying a respective
8 number of signal vias and a respective number of return current paths for a
9 plurality of cells in a grid of a set cell size within said identified design layout;
10 calculating ratio of signal vias to return current paths for each of said
11 plurality of cells;
12 identifying each cell having said calculated ratio greater than a target
13 ratio; and
14 selectively adding one or more decoupling capacitors within each said
15 identified cell for providing high frequency return current paths.

1 12. A computer program product for implementing high frequency
2 return current paths as recited in claim 11 wherein the step of receiving
3 electronic package physical design data for identifying said board layout
4 includes the steps of receiving plane stack-up data for identifying reference
5 voltages residing on multiple planes and for creating pairs of reference
6 voltages to be analyzed.

1 13. A computer program product for implementing high frequency
2 return current paths as recited in claim 11 wherein the step of receiving
3 electronic package physical design data for identifying said board layout
4 includes the steps of receiving a board file for identifying locations of high
5 speed nets, locations of plane change vias, and board dimensions.

1 14. A computer program product for implementing high frequency
2 return current paths as recited in claim 11 includes the steps of receiving a
3 user selected value for said target ratio; said target ratio defining a maximum
4 desired ratio of signal vias to return current paths; and receiving a user
5 selected grid dimensions input defining said set cell size.

1 15. A computer program product for implementing high frequency
2 return current paths as recited in claim 11 wherein the step of selectively
3 adding one or more decoupling capacitors within each said identified cell for
4 providing high frequency return current paths includes the steps of
5 calculating a capacitance value, a capacitor quantity, and optimal placement
6 for adding said one or more decoupling capacitors within said cell.

1 16. A computer program product for implementing high frequency
2 return current paths as recited in claim 11 wherein the step of selectively
3 adding one or more decoupling capacitors within each said identified cell for
4 providing high frequency return current paths includes the steps of
5 identifying nets referenced to at least one reference voltage within each said
6 identified cell; and connecting said one or more decoupling capacitors
7 between at least one ground plane and at least one plane for said at least
8 one reference voltage within said cell.

1 17. Apparatus for implementing high frequency return current
2 paths utilizing decoupling capacitors within electronic packages comprising:
3 a return path analyzer computer program for receiving electronic
4 package physical design data for identifying a design layout; utilizing said
5 identified design layout for identifying a respective number of signal vias and
6 a respective number of return current paths for a plurality of cells in a grid of
7 a set cell size within said identified design layout; and for calculating ratio of
8 signal vias to return current paths for each of said plurality of cells;
9 a capacitor calculation tool computer program for identifying each cell
10 having said calculated ratio greater than a target ratio; and for selectively
11 adding one or more decoupling capacitors within each said identified cell for
12 providing high frequency return current paths.

1 18. Apparatus for implementing high frequency return current
2 paths as recited in claim 17 wherein said electronic package physical design
3 data include plane stack-up data used by said return path analyzer computer
4 program for identifying reference voltages residing on multiple planes and for
5 creating pairs of reference voltages to be analyzed.

1 19. Apparatus for implementing high frequency return current
2 paths as recited in claim 17 wherein said electronic package physical design
3 data include a board file used by said return path analyzer computer
4 program for identifying locations of high speed nets, locations of plane
5 change vias, and board dimensions.

1 20. Apparatus for implementing high frequency return current
2 paths as recited in claim 17 wherein said return path analyzer computer
3 program receives a user selected value for said target ratio; said target ratio
4 defining a maximum desired ratio of signal vias to return current paths; and
5 receives a user selected grid dimensions input defining said set cell size.